library IEEE;

use IEEE.STD\_LOGIC\_1164.ALL;

use ieee.numeric\_std.all;

entity part\_2 is

generic(SAM\_SIZE:integer:=8;

OUT\_SIZE:integer:=16;

FAC\_SIZE:integer:=8);

Port ( p\_0, p\_1:in std\_logic\_vector(SAM\_SIZE-1 downto 0) ;

alpha:in std\_logic\_vector(FAC\_SIZE-1 downto 0);

p\_f:out std\_logic\_vector(OUT\_SIZE-1 downto 0);

clk:in std\_logic

);

end part\_2;

architecture Behavioral of part\_2 is

--CLK WIZARD

component clk\_wiz\_0

port

(-- Clock in ports

-- Clock out ports

clk\_out1 : out std\_logic;

clk\_out2 :out std\_logic;

-- Status and control signals

locked : out std\_logic;

clk\_in1 : in std\_logic

);

end component;

signal s0, s1 :std\_logic\_vector(SAM\_SIZE-1 downto 0);

signal blend:std\_logic\_vector(OUT\_SIZE-1 downto 0):="0000000000000000";

signal locked,clk1x,clk2x:std\_logic;

signal temp2, temp3, temp4:signed(OUT\_SIZE-1 downto 0);

signal temp0, temp1:signed(SAM\_SIZE-1 downto 0);

begin

u1:clk\_wiz\_0 port map(clk\_out1=>clk1x, clk\_out2=>clk2x, locked=>locked, clk\_in1=>clk);

data\_in:process(clk1x)

begin

if rising\_edge(clk1x) then

s0 <=p\_0;

s1<=p\_1;

end if;

end process;

multiplication:process(clk2x)

variable var0, var1,var2:signed(SAM\_SIZE-1 downto 0);

variable var3,var4,var5:signed(OUT\_SIZE-1 downto 0);

begin

if clk2x'event and clk2x='1' then

var0:=signed(s0);

temp0<=var0;

var1:=signed(alpha);

temp1<=var1;

var3:=temp0\*temp1;

temp2<=var3;

else

var0:=signed(s1);

temp0<=var0;

var1:=to\_signed(127,8)-signed(alpha);

temp1<=var1;

var3:=temp0\*temp1;

temp2<=var3;

end if;

end process;

add:process(clk2x)

variable var0 :signed(OUT\_SIZE-1 downto 0);

begin

if clk2x'event and clk2x='1' then

temp4<=temp2+0;

else

temp4<=temp4+temp2;

end if;

end process;

data\_out:process(clk1x)

begin

if rising\_edge(clk1x) then

p\_f<=std\_logic\_vector(temp4);

end if;

end process;

end Behavioral;

library IEEE;

use IEEE.STD\_LOGIC\_1164.ALL;

use ieee.numeric\_std.all;use IEEE.STD\_LOGIC\_1164.ALL;

use ieee.std\_logic\_unsigned.all;

entity tb\_part\_1 is

generic (DI\_SIZE:integer :=8;

DO\_SIZE:integer :=16);

end tb\_part\_1;

architecture Behavioral of tb\_part\_1 is

--component part\_1

--Port ( p\_0, p\_1:in std\_logic\_vector(8 downto 0) ;

-- alpha:in std\_logic\_vector(7 downto 0);

-- p\_f:out std\_logic\_vector(15 downto 0));

--end component;

component part\_2

Port ( p\_0, p\_1:in std\_logic\_vector(7 downto 0) ;

alpha:in std\_logic\_vector(7 downto 0);

p\_f:out std\_logic\_vector(15 downto 0);

clk:in std\_logic);

end component;

constant clock\_period:time:=20 ns;

signal clk:std\_logic;

signal p\_0, p\_1:std\_logic\_vector(DI\_SIZE-1 downto 0);

signal p\_f :std\_logic\_vector(DO\_SIZE-1 downto 0);

signal alpha:std\_logic\_vector(DI\_SIZE-1 downto 0);

begin

clock:process

begin

clk<='0';

wait for clock\_period/2;

clk<= not clk;

wait for clock\_period/2;

end process;

sine\_wave\_inputs :process

begin

p\_0 <= std\_logic\_vector(to\_signed(0,DI\_SIZE));

p\_1 <= std\_logic\_vector(to\_signed(0,DI\_SIZE));

wait for 12.5 ns;

p\_0 <= std\_logic\_vector(to\_signed(75,DI\_SIZE));

p\_1 <= std\_logic\_vector(to\_signed(37,DI\_SIZE));

wait for 12.5 ns;

p\_0 <= std\_logic\_vector(to\_signed(121,DI\_SIZE));

p\_1 <= std\_logic\_vector(to\_signed(60,DI\_SIZE));

wait for 12.5 ns;

p\_0 <= std\_logic\_vector(to\_signed(121,DI\_SIZE));

p\_1 <= std\_logic\_vector(to\_signed(60,DI\_SIZE));

wait for 12.5 ns;

p\_0 <= std\_logic\_vector(to\_signed(75,DI\_SIZE));

p\_1 <= std\_logic\_vector(to\_signed(37,DI\_SIZE));

wait for 12.5 ns;

p\_0 <= std\_logic\_vector(to\_signed(0,DI\_SIZE));

p\_1 <= std\_logic\_vector(to\_signed(0,DI\_SIZE));

wait for 12.5 ns;

p\_0 <= std\_logic\_vector(to\_signed(-75,DI\_SIZE));

p\_1 <= std\_logic\_vector(to\_signed(-37,DI\_SIZE));

wait for 12.5 ns;

p\_0 <= std\_logic\_vector(to\_signed(-121,DI\_SIZE));

p\_1 <= std\_logic\_vector(to\_signed(-60,DI\_SIZE));

wait for 12.5 ns;

p\_0 <= std\_logic\_vector(to\_signed(-121,DI\_SIZE));

p\_1 <= std\_logic\_vector(to\_signed(-60,DI\_SIZE));

wait for 12.5 ns;

p\_0 <= std\_logic\_vector(to\_signed(-75,DI\_SIZE));

p\_1 <= std\_logic\_vector(to\_signed(-37,DI\_SIZE));

end process;

alpha\_input:process

begin

alpha <= std\_logic\_vector(to\_signed(0,8));

wait for 5000 ns;

alpha <= std\_logic\_vector(to\_signed(127,8));

wait for 5000 ns;

end process;

--u1:part\_1 port map(p\_0=>p\_0, p\_1=>p\_1, alpha=>alpha, p\_f=>p\_f);

u2:part\_2 port map(p\_0=>p\_0, p\_1=>p\_1, alpha=>alpha, p\_f=>p\_f, clk=>clk);

end Behavioral;